

AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth in the following listing. This listing of claims will replace all prior versions, and listings, of claims for the present application:

Claims 1 - 5 (Previously Canceled).

6. (Previously Presented) A semiconductor device formed using a photo-definable layer in a positive mask scheme, comprising:

a substrate; and

at least one feature formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a positive mask scheme and by using non-exposed portions of said photo-definable layer as a mask to form said at least one feature.

7. (Previously Presented) The semiconductor device of claim 6, further comprising an insulative layer formed on said substrate from said non-exposed portions of said photo-definable layer that were subsequently converted to an insulative layer through exposure to electro-magnetic radiation.

8. (Previously Presented) The semiconductor device of claim 7, wherein said photo-definable layer comprises an organosilicon resist.

9. (Previously Presented) The semiconductor device of claim 8, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

10. (Previously Presented) The semiconductor device of claim 9, wherein said feature is part of a memory cell array.

Claims 11-18 (Previously Canceled).

19. (Previously Presented) A patterned insulative structure within a semiconductor device formed using a photo-definable layer in a positive mask scheme, comprising:

a substrate; and

a patterned insulative layer formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electromagnetic radiation in a positive mask scheme and by using non-exposed portions of said photo-definable layer as a mask to form said patterned insulative layer.

20. (Previously Presented) The patterned insulative structure of claim 19, wherein said insulative layer comprises an oxide layer.

21. (Previously Presented) The patterned insulative structure of claim 20, wherein said photo-definable layer comprises an organosilicon resist.

22. (Previously Presented) The patterned insulative structure of claim 21, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

23. (Previously Presented) The patterned insulative structure of claim 22, wherein said insulative layer comprises a plurality of trench structures within a memory cell array.

24. (Previously Presented) The patterned insulative structure of claim 23, wherein said patterned insulative layer comprises non-exposed portions of said photo-definable layer that were converted into additional insulative material after formation of said patterned insulative layer.

Claims 25 - 33 (Previously Canceled).

34. (Previously Presented) A conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising:

a substrate;

a first conductive layer over said substrate;

an insulative layer over said conductive layer; and

a second conductive layer formed within a desired portion of said insulative layer to create a conductive interconnect structure connected to said first conductive layer, said second conductive layer being formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electromagnetic radiation in a positive mask scheme, by using non-exposed portions of said photo-definable layer as a mask to form a pattern within said insulative layer, and by using non-exposed portions of said photo-definable layer as a sacrificial mask in etching said second conductive layer.

35. (Previously Presented) The conductive interconnect structure of claim 34, wherein said photo-definable layer comprises an organosilicon resist.

36. (Previously Presented) The conductive interconnect structure of claim 35, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

37. (Previously Presented) The conductive interconnect structure of claim 34, wherein said substrate includes a plurality of transistor gate structures for a memory cell array.

Claims 38 - 48 (Previously Canceled).

49. (Previously Presented) A patterned insulative structure within a semiconductor device using a photo-definable layer as a mask layer, comprising:

a substrate; and

an insulative layer on said substrate formed by covering a photo-definable layer with a patterned organic photoresist, by converting unmasked portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a positive mask scheme, and by using non-exposed portions of said photo-definable layer and said organic photoresist as a mask to form a pattern within said insulative layer.

50. (Previously Presented) The patterned insulative structure of claim 49, wherein said photo-definable layer comprises an organosilicon resist.

51. (Previously Presented) The patterned oxide structure of claim 50, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

52. (Previously Presented) The patterned insulative structure of claim 51, wherein said insulative layer comprises an oxide layer.

53. (Previously Presented) The patterned insulative structure of claim 52, wherein said insulative layer comprises a plurality of trench structures within a memory cell array.

54. (Previously Presented) The patterned insulative structure of claim 49, wherein said insulative layer comprises non-exposed portions of said photo-definable layer subsequently converted into additional insulative material.

Claims 55 - 100 (Canceled).